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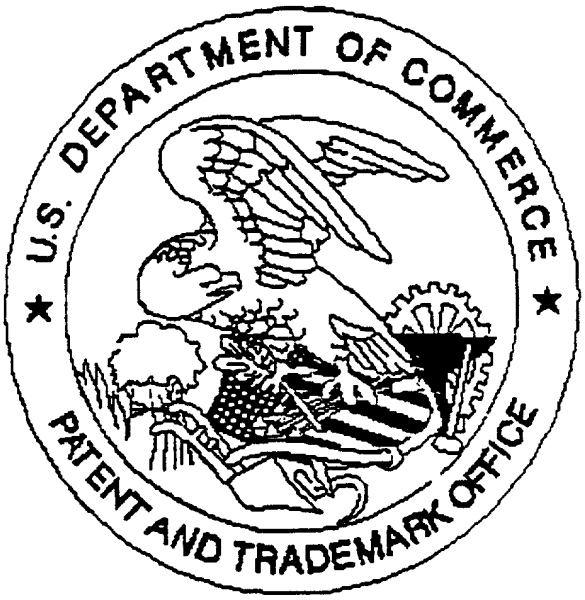

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FIG. 3 illustrates interference mechanisms among the various blocks of an RF transceiver. The embodiments of the invention in FIGS. 2A-2D, depicting RF transceivers partitioned according to the invention, seek to overcome, reduce, or minimize those interference mechanisms.

FIG. 4 shows a more detailed block diagram of RF transceiver circuitry partitioned according to the invention.

FIG. 5 illustrates an alternative technique for partitioning RF transceiver circuitry.

FIG. 6 shows yet another alternative technique for partitioning RF transceiver circuitry.

FIG. 7 depicts a more detailed block diagram of RF transceiver circuitry partitioned according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 8 illustrates a more detailed block diagram of a multi-band RF transceiver circuitry partitioned according to the invention.

FIG. 9A shows a block diagram of an embodiment of the interface between the receiver digital circuitry and receiver analog circuitry in an RF transceiver according to the invention.

FIG. 9B depicts a block diagram of another embodiment of the interface between the baseband processor circuitry and the receiver analog circuitry in an RF transceiver according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 10 illustrates a more detailed block diagram of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a serial interface.

FIG. 11A shows a more detailed block diagram of an embodiment of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a data and clock signal interface.

FIG. 11B illustrates a block diagram of an embodiment of a delay-cell circuitry that includes a clock driver circuitry in tandem with a clock receiver circuitry.

FIG. 12 depicts a schematic diagram of an embodiment of a signal-driver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

FIG. 13 illustrates a schematic diagram of an embodiment of signal-receiver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.